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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Nils Endric Schubert, et al.

Application No: 09/724,839

Filed: November 28, 2000

For: Design Instrumentation Circuitry

Examiner: Yolanda L. Wilson

Art Unit: 2184

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CONCISE EXPLANATION UNDER 37 C.F.R. 1.98(3)(i)

Dear Sir:

It is respectfully requested that the Concise Explanation of the German article by Haufe, M., et al., entitled, "Ein Debugger für ASIC-Prototypen", enclosed herewith and named in attached Information Disclosure Statement be entered:

FIRST CLASS CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 March 8, 2004
Date of Deposit

Carla Vignola
Name of Person Mailing Correspondence

Signature

3-8-04
Date

Listing of the German Article:

1. "Ein Debugger fuer ASIC-Prototypen", DASS
Dresden Germany, 2000 by J. Haufe

Abstract: FPGA-based ASIC prototyping enables verification and debugging of the ASIC design. The key advantage of FPGA-based prototyping is performance. The drawback is the lack of software tools for analyzing and debugging of the FPGA prototype. This presentation shows how a Hardware Debugger for FPGA-based prototyping can be built

Slide 1: Title and Authors

Slide 2: Outline of the talk: Motivation, requirements, architecture of a hardware debugger, hardware debugger components, designflow, outlook.

Slide 3: Current approaches are not sufficient. State-of-the-art methods for hardware debugging: external test pins and logic analyzers; long simulation runs, partially at gate-level. Designer need real-time performance and internal visibility.

Slide 4: Requirements for hardware debuggers: Device-under-test runs at real-time speed, no adverse impact on DUT timing, real-time traces and breakpoints, independent of target technology, controllable via host computer, compatible with standard design flows, plug-and-play capable.

Slide 5: First application: Trace method. Start simulation run from hardware-obtained traces to save simulation time.

Slide 6: Second application: Start hardware debugging run off of simulation values.

Slide 7: Architecture of a hardware debugger. Shadow the registers in DUT with trace registers in the hardware debugger to obtain internal visibility.

Slide 8: Architecture of a hardware debugger. Separate hardware for the hardware debugger connected to trace/update circuitry in the DUT via serial interface. Slow but low area overhead in DUT.

Slide 9: Architecture of a hardware debugger. Integrate hardware debugger into DUT. Fast but high area overhead.

Slide 10: Put hardware debugger kernel into DUT, leave most hardware debugger components outside of DUT on separate board. Optimum performance with best possible area overhead.

Slide 11: Circuitry to implement a shadow register for storing trace information.

Slide 12: Implementation of gate-level breakpoint circuitry via VHDL code insertions.

Slide 13: Implementation of a hardware debugger kernel as a finitew statemachine.

Slide 14: Implementation of a debugger interface.

Slide 15: Design flow for using hardware debugger approach. Insertion of breakpoints at RTL and/or gate-level, insertion of shadowcells at gate-level, hook-up of hardware debug kernel. Switching between simulation and hardware debugging.

Slide 16: Outlook: This approach enables observing and modification of all registers, technology independent, capable of running at real-time. Drawback: Needs additional components in the prototype, needs additional pins, no back-annotation of trace data to RTL, no support of embedded RAM, works only on single clock systems, no continuous signal tracing possible.

Slide 17: Applications to debugging of prototypes, data logging, error emulation, temporary changes of the design, forced state changes in circuit registers, IP-Core test within the circuit, basic software debugger for processor cores.

COMMENTS

In compliance with 37 C.F.R. 1.98(3)(i), the foregoing concise explanation is an explanation of the relevance, as it is presently understood by the individual designated most knowledgeable about the content of the information listed that is not in the English language. The Applicant has provided the slide numbers together with its relevance of the German article.

CONCLUSION

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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